San José State University
Electrical Engineering Department
EE-227, Signal Integrity in AMS IC

Course and Contact Information

Instructor: Dr. Shahab Ardalan

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Office Hours: TBD

Class Days/Time: TBD

Classroom: TBD

Course Website: http://www.engr.sjsu.edu/ardalan

Course Description

This course studies essential blocks for wire-line communication integrated circuits such as analog equalizer circuits, Decision-Feedback Equalization (DFE), Phase Looked Loop (PLL) and Clock and Data Recovery (CDR) circuits. True understanding of system level modeling and behavioral of the PLL will be discussed. Matlab/Simulink Modeling techniques will be introduced as new vehicle for system level design and simulation. Performance metrics such as random jitter, BER, jitter transfer jitter tolerance, phase noise and … will be introduced. Integrated circuit design consideration for the key essential blocks for PLL and equalizer block will be covered

Course Learning Outcomes

Upon successful completion of this course, students will be able to:

CLO 1. Understanding equalization concept in wire-line communication circuits.
CLO 2. Understanding phase locking techniques and clock and data recovery concepts.
CLO 3. Understanding performance metrics such as Jitter tolerance, Jitter transfer, Jitter peaking, random jitter, phase noise, BER and …
CLO 4. The ability to model equalizer, PLL and CDR using Matlab/Simulink

CLO 5. The ability to design essential circuit block for data communication such as phase detectors, charge pump, loop-filter, Ring and LC-tank voltage controlled oscillators, boosting filters, DC restoration.
CLO 6. Understanding mechanism and procedures for testing a phase locked loop

Required Texts/Readings

Textbook

1. *Instructor Notes*
2. *"Design of Integrated Circuits for Optical Communications", B. Razavi, Wiley, 2012, ISBN-10: 1118336941, ISBN-13: 978-1118336946*

Other Readings

"Phase-Locking in High Performance Systems from Devices to Architectures", B. Razavi, IEEE Press, 2003 (Available on IEEE Explorer)

Course Requirements and Assignments

Class participation, assignments, midterm exam, design project and final exam

Grading Policy

Exams will be closed book. However, students are allowed to bring 1/2 page of aid sheet, where can be option from this link (www.ardalan.ws/pdf). There will be no make-up exam and those absent will receive no credit. Students must write their answers clearly in an organized fashion. Further instructions will be provided during exams. The course is based on letter grading and grading percentage breakdown is as follow:

90% and above A
89% - 85% A-
84% - 82% B+
81% - 79% B
78% - 75% B-
74% - 72% C+
71% - 69% C
68% - 65% C-
64% - 62% D+
61% - 59% D
58% - 55% D
below 55% F

Total final grade is

Assignment	5%
Mid-term Exam	25%
Design Project	30%
Final Exam	40%

Design Project:

Projects are mainly based on system level modeling in Simulink and circuit implementation on Cadence and are closely relate to topics discussed in this course. Cadence will not be taught in this course and students are required to master this CAD tool by themselves. However the cadence tutorial is available on the course website. Each group (maximum 3 students) must write a formal project report using a word processor (i.e. Microsoft Office) and submit the original write-up

Classroom Protocol

Students are required to be in class on time and no use of cell phone during the class.

University Policies

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Refer to the current semester's Catalog Policies section at http://info.sjsu.edu/static/catalog/policies.html. Add/drop deadlines can be found on the current academic year calendars document on the Academic Calendars webpage at http://www.sjsu.edu/provost/services/academic_calendars/. The Late Drop Policy is available at http://www.sjsu.edu/aars/policies/latedrops/policy/**.** Students should be aware of the current deadlines and penalties for dropping classes.

Information about the latest changes and news is available at the Advising Hub at http://www.sjsu.edu/advising/.

Consent for Recording of Class and Public Sharing of Instructor Material

- "Common courtesy and professional behavior dictate that you notify someone when you are recording him/her. You must obtain the instructor's permission to make audio or video recordings in this class. Such permission allows the recordings to be used for your private, study purposes only. The recordings are the intellectual property of the instructor; you have not been given any rights to reproduce or distribute the material." To obtain the permission for recording the lectures you need to request it in formal writing for each lecture.
- "Course material developed by the instructor is the intellectual property of the instructor and cannot be shared publicly without his/her approval. You may not publicly share or upload instructor generated material for this course such as exam questions, lecture notes, or homework solutions without instructor consent."

Academic integrity

Your commitment, as a student, to learning is evidenced by your enrollment at San Jose State University. The University Academic Integrity Policy S07-2 at http://www.sjsu.edu/senate/docs/S07-2.pdf requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The Student Conduct and Ethical Development website is available at http://www.sjsu.edu/studentconduct/.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 at

http://www.sjsu.edu/president/docs/directives/PD_1997-03.pdf requires that students with disabilities requesting accommodations must register with the Accessible Education Center (AEC) at http://www.sjsu.edu/aec to establish a record of their disability.

Accommodation to Students' Religious Holidays

San José State University shall provide accommodation on any graded class work or activities for students wishing to observe religious holidays when such observances require students to be absent from class. It is the responsibility of the student to inform the instructor, in writing, about such holidays before the add deadline at the start of each semester. If such holidays occur before the add deadline, the student must notify the instructor, in writing, at least three days before the date that he/she will be absent. It is the responsibility of the instructor to make every reasonable effort to honor the student request without penalty, and of the student to make up the work missed. See University Policy S14-7 at http://www.sjsu.edu/senate/docs/S14-7.pdf.

EE227-Signal Integrity in AMS IC, Course Schedule

Course Schedule

Date	Topic
24-Aug-15	Introduction to wire-line communication
26-Aug-15	Introduction to equalization and phase locking concept
31-Aug-15	Phase Detectors
02-Sep-15	Current Mode Logic
07-Sep-15	Labor Day
09-Sep-15	Phase Locked Loop- System level
14-Sep-15	Phase Locked Loop- Analog type-1
16-Sep-15	Phase Locked Loop- Analog type-2
21-Sep-15	Non-Linear Phase Locking-1
23-Sep-15	Non-Linear Phase Locking-2 (CDR)
28-Sep-15	Phase Detector Modeling in Simulink
30-Sep-15	Clock, Data Source and VCO modeling in Simulink
05-Oct-15	Linear PLL Modeling in Simulink
07-Oct-15	Non-Linear PLL Modeling in Simulink
12-Oct-15	Review
14-Oct-15	Mid Term
19-Oct-15	Performance Metrics-1
21-Oct-15	Performance Metrics-1
26-Oct-15	Introduction to Oscillation
28-Oct-15	LC Based VCO
02-Nov-15	Ring VCO, Phase Noise in VCOs
04-Nov-15	Phase Noise Modeling in Simulink
09-Nov-15	Advanced CDR Architectures-1 (Clock FWD, Embedded Clock, Delay Locked Loop)
11-Nov-15	Advanced CDR Architectures-2 (Phase Interpolation)
16-Nov-15	Advanced CDR Architectures-3 (Lock Injection)
18-Nov-15	Dual Loop Architectures
23-Nov-15	Digital PLL-1
25-Nov-15	Digital PLL-2
30-Nov-15	Analog Equalization and DFE
02-Dec-15	Project Demo
07-Dec-15	Project Presentation 1
09-Dec-15	Project Presentation 2